PROJ200 Group Project

Title

Group: M

Names:

A. Owen Fiddy

B. Mobashirul Karim

C. Michael Keefe

D. Kien Phan

Date: n/a

Table of Contents

[1. Analogue Circuit Design & Simulation 3](#_Toc160434826)

[1.1 Bandpass filter cutoff 3](#_Toc160434827)

[1.2 Gain 3](#_Toc160434828)

[1.3 Simulation 3](#_Toc160434829)

[1.4 PCB Design 3](#_Toc160434830)

[2. Signal Sampling (FPGA) 3](#_Toc160434831)

[2.1 HDL code circuit description 3](#_Toc160434832)

[2.2 Test benches 3](#_Toc160434833)

[3. Real-Time Software 3](#_Toc160434834)

[3.1 Heart Rate Calculation algorithm 3](#_Toc160434835)

[3.2 Sample rate 3](#_Toc160434836)

[3.3 Display Rate 3](#_Toc160434837)

[3.3 SPI 3](#_Toc160434838)

[4.Testing 4](#_Toc160434839)

[4.1 Bandwidth measurement 4](#_Toc160434840)

[4.2 SPI Waveform 4](#_Toc160434841)

[4.3 Oscilloscope waveform 4](#_Toc160434842)

[4.4 Sampled Data Waveform 4](#_Toc160434843)

[4.5 LCD Display 4](#_Toc160434844)

[5. Results 4](#_Toc160434845)

[6. Conclusions 4](#_Toc160434846)

[APPENDIX 5](#_Toc160434847)

# 1. Analogue Circuit Design & Simulation

* Max 2 Pages
* Calculations  showing

## 1.1 Bandpass filter cutoff

## 1.2 Gain

## 1.3 Simulation

* (Bandwidth Graph & Voltages at test points)

## 1.4 PCB Design

* (showing component values and test points)

# 2. Signal Sampling (FPGA)

* Max 2 Pages

## 2.1 HDL code circuit description

## 2.2 Test benches

* (annotated timing diagram and automated tests)
* You need to evidence that the signal is sampled evenly, at the correct rate, and that no samples are dropped or corrupted.  Develop and describe your methodology for both **verification** and **validation**.
* For verification, you should write testbenches for each of your components and present the results. For validation, consider using a signal generator and SignalTap (or another method of your own design).

# 3. Real-Time Software

* Max 2 Pages
* C code flowchart or pseudocode for main program and what each function does

## 3.1 Heart Rate Calculation algorithm

## 3.2 Sample rate

## 3.3 Display Rate

## 3.3 SPI

* Sample rate vs Display rate
* Any averaging to remove errors
* Data from the FPGA shall be transferred to the MCU for analysis using the provided SPI interface. The timing of this needs to be synchronised such that no data is lost and risk of metastability is minimised. You should aim to evenly spread the CPU loading over time.
* You will need to describe your software technique to achieve this.
* You also need to present both methodology and test results to evidence correct functionality.

# 4.Testing

* Max 4 pages

## 4.1 Bandwidth measurement

* (Graph) overlayed on Simulation vs Measured bandwidth response

## 4.2 SPI Waveform

* Data waveform from SPI showing ADC data

## 4.3 Oscilloscope waveform

* showing peaks and time measured and rate calculated by your system.

## 4.4 Sampled Data Waveform

* Testing data to determine sample points and peak timing form pulses

## 4.5 LCD Display

* What is shown on output LCD display

# 5. Results

* Max 2 page
* Explain differences between simulation and measured performance
* How accurate is the pulse measurements and the output to LCD
* Provide information on the accuracy and reliability of the final system.
* This should include including measurement errors due to sampling and quantisation.
* Comment on the impact of noise and distortion.

# 6. Conclusions

* Max 1 page
* How well did your system perform?
* Quantitative vs Qualitative (measurements vs good/bad) what would you expect? Is it accurate enough? How could you improve it?
* Critically report on the limitations of your validation technique.

## APPENDIX

* No Page Limit, No Marks
* Task List – Completed by
  + Bandpass design & Simulation
  + PCB Design
  + HDL Code test benches
  + Real-Time Software main & functions
  + Testing
  + Results
  + Conclusion

HDL Test Benches

Code

Test Data